

TFT LCD Approval Specification

MODEL NO.: R190E1-L01

Customer: _____

Approved by: _____

Note:

記錄	工作	審核	角色	投票
2007-11-21 16:28:26 CST	PMMD Director	kj_cheng(鄭光容 /56505/54419/14107)	Director	Accept

- CONTENTS -

REVISION HISTORY	-----	3
1. GENERAL DESCRIPTION	-----	4
1.1 OVERVIEW		
1.2 FEATURES		
1.3 APPLICATION		
1.4 GENERAL SPECIFICATIONS		
1.5 MECHANICAL SPECIFICATIONS		
2. ABSOLUTE MAXIMUM RATINGS	-----	5
2.1 ABSOLUTE RATINGS OF ENVIRONMENT		
2.2 ELECTRICAL ABSOLUTE RATINGS		
2.2.1 TFT LCD MODULE		
2.2.2 BACKLIGHT UNIT		
3. ELECTRICAL CHARACTERISTICS	-----	6
3.1 TFT LCD MODULE		
3.2 BACKLIGHT UNIT		
3.3 Inverter Electrical characteristic		
4. BLOCK DIAGRAM	-----	11
4.1 TFT LCD MODULE		
4.2 BACKLIGHT UNIT		
5. INPUT TERMINAL PIN ASSIGNMENT	-----	12
5.1 TFT LCD MODULE		
5.2 LVDS Input Data Order		
5.3 Inverter Input Signal		
5.4 COLOR DATA INPUT ASSIGNMENT		
6. INTERFACE TIMING	-----	14
6.1 INPUT SIGNAL TIMING SPECIFICATIONS		
6.2 POWER ON/OFF SEQUENCE		
7. OPTICAL CHARACTERISTICS	-----	16
7.1 OPTICAL SPECIFICATIONS		
8. PACKAGING	-----	19
8.1 PACKING SPECIFICATIONS		
8.2 PACKING METHOD		
9. DEFINITION OF LABELS	-----	21
10. PRECAUTIONS	-----	22
10.1 ASSEMBLY AND HANDLING PRECAUTIONS		
10.2 SAFETY PRECAUTIONS		
11. MECHANICAL CHARACTERISTICS	-----	23

REVISION HISTORY

Version	Date	Section	Description
Ver 0.0	Dec, 15, '06	All	R190E1 -L01 Specification was first issued.
Ver 0.1	Jan, 02, '07	5.2	Replace "Backlight Unit" by "Inverter Input Signal"
Ver 2.0	Nov.,16, '07	1.5	Max. Weight Specification Update, 2100 to 2050 g
		3.3	Specification Update, Item 1, 2,3,8
			New Added, VDIM vs Dimming Range Chart
		5.1	New Added, Note 4
		8.2	Package Method updated

1. GENERAL DESCRIPTION

1.1 OVERVIEW

R190E1-L01 is an 19.0" TFT Liquid Crystal Display module with 16 CCFL Backlight unit and 30 pins and one port 2ch-LVDS interface. This module supports 1280 x 1024 SXGA mode and can display 16.7M colors driven by 8bit drivers. The LCD module includes built-in inverter for Backlight.

1.2 FEATURES

This specification applies to the Type 19.0" Color TFT LCD Module, Model R190E1-L01

- This module includes an inverter card for the backlight.
- The screen format is intended to support SXGA 1280(H)x1024(V) resolution.
- Supported colors are native 16M (8-bits data per R, G, B each).
- All input signals are LVDS (Low Voltage Differential Signaling) interface.
- The contrast was enhanced to enable gray scale application

1.3 APPLICATION

- This module is designed for a TFT LCD Monitor style display unit.

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	376.32 (H) x 301.056 (V) (19.0" diagonal)	mm	(1)
Bezel Opening Area	380.2(H) x 305(V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1280 x R.G.B. x 1024	pixel	-
Pixel Pitch	0.294 (H) x 0.294 (V)	mm	-
Pixel Arrangement	RGB vertical stripe (at landscape position)	-	-
Display Colors	16.7M (8-bits data per R, G, B each)	color	-
Display Mode	Normally Black	-	-
Surface Treatment	Hard coating (3H), Anti-glare (Haze 25)	-	-

1.5 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	403.7	404.2	404.7	(1)
	Vertical(V)	329.5	330.0	330.5	
	Depth(D)	34.7	35.2	35.7	
Weight	-	-	2050	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	+50	°C	(1), (2)
Shock (Non-Operating)	S _{NOP}	-	50	G	(3), (5)
Vibration (Non-Operating)	V _{NOP}	-	1.5	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≤ 40 °C).

(b) Wet-bulb temperature should be 39 °C Max. (Ta > 40 °C).

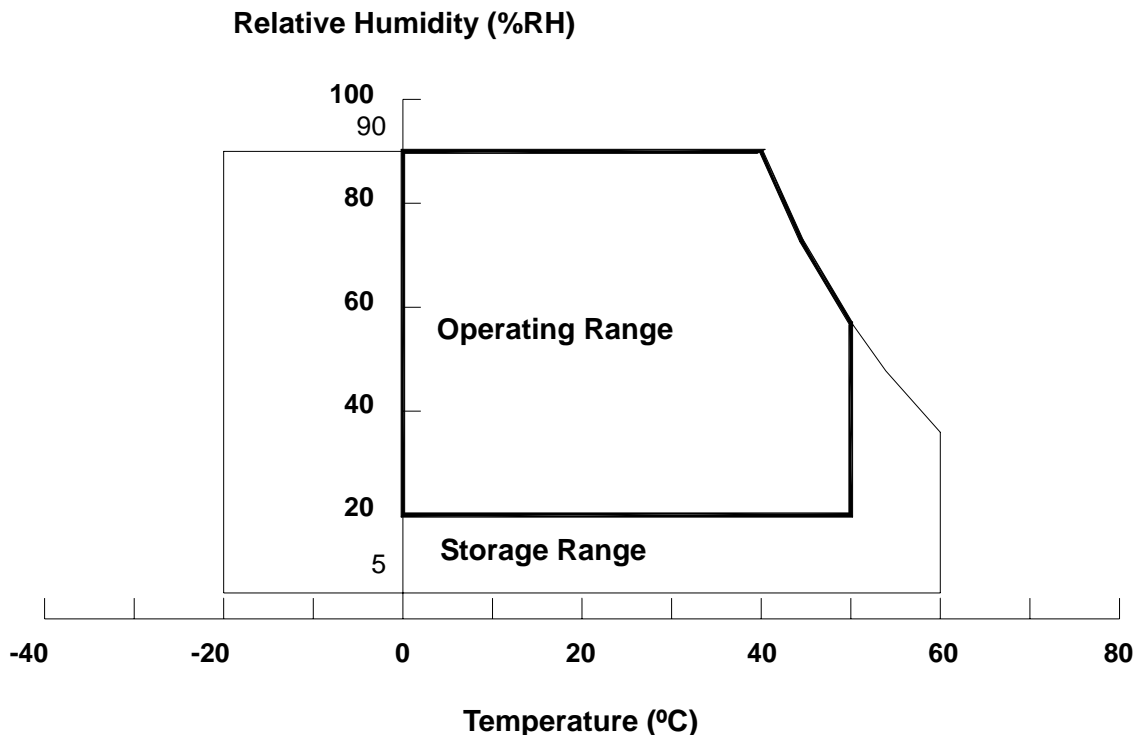
(c) No condensation.

Note (2) The temperature of panel display surface area should be 0 °C Min. and 60 °C Max.

Note (3) 11ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 300 Hz, 10min/cycle, 3 cycles each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V _{CC}	-0.3	+6.0	V	(1)

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V _L	-	2.5K	V _{RMS}	(1), (2)
Lamp Current	I _L	-	7	mA _{RMS}	(1), (2)
Lamp Frequency	F _L	-	80	KHz	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to 3.2 for further information).

3. ELECTRICAL CHARACTERISTICS

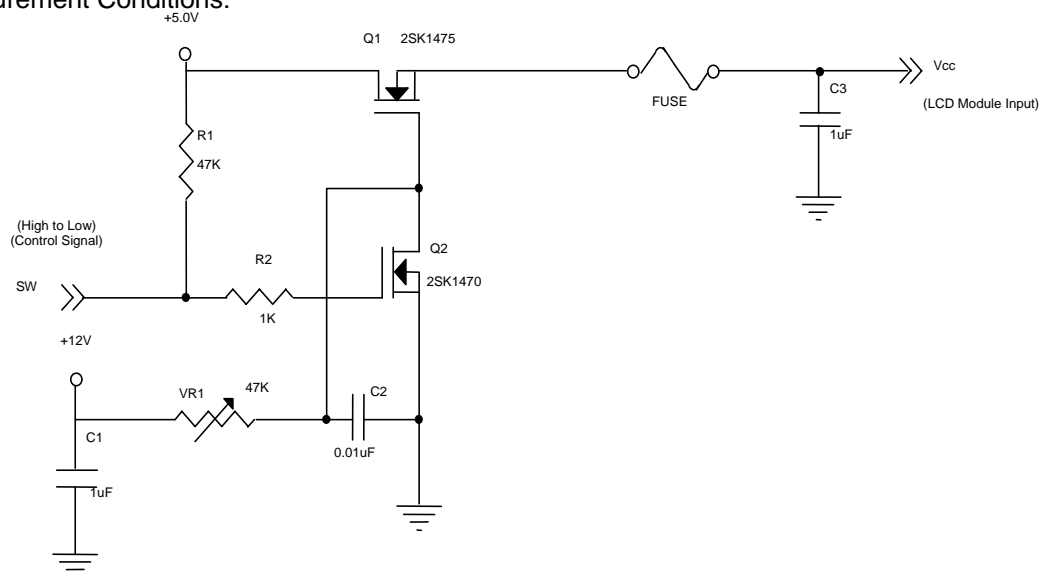
3.1 TFT LCD MODULE

T_a = 25 ± 2 °C

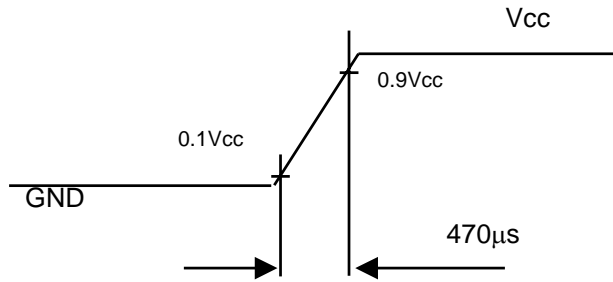
Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Supply Voltage	V _{CC}	4.5	5.0	5.5	V	-
Ripple Voltage	V _{RP}	-	-	100	mV	-
Rush Current	I _{RUSH}	-	-	3.8	A	(2)
Power Supply Current	White	-	1080	1500	mA	(3)a
	Black	-	650	900	mA	(3)b
	Vertical Stripe	-	1020	1500	mA	(3)c
LVDS differential input voltage	V _{id}	-100	-	+100	mV	
LVDS common input voltage	V _{ic}	-	1.2	-	V	

Note (1) The module is recommended to operate within specification ranges listed above for normal function.

Note (2) Measurement Conditions:

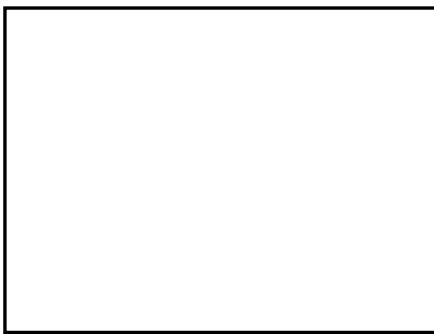


Vcc rising time is 470 μ s



Note (3) The specified power supply current is under the conditions at Vcc = 5.0 V, Ta = 25 \pm 2 $^{\circ}$ C, fv = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern



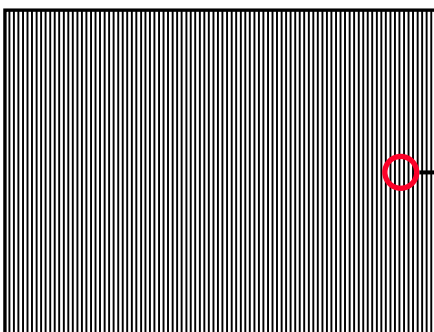
Active Area

b. Black Pattern

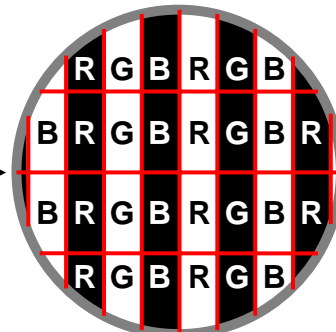


Active Area

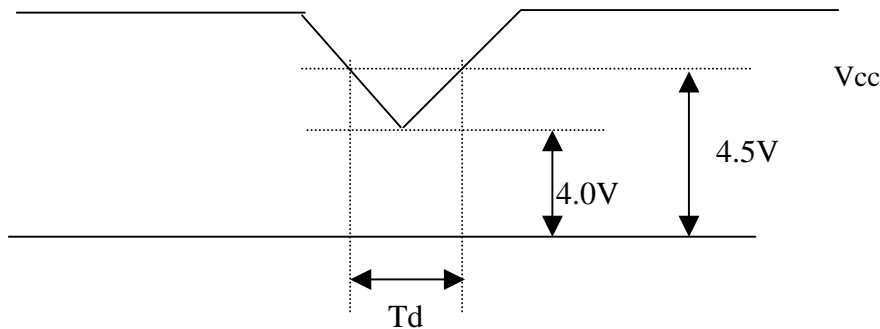
c. Vertical Stripe Pattern



Active Area



3.2 Vcc POWER DIP CONDITION:



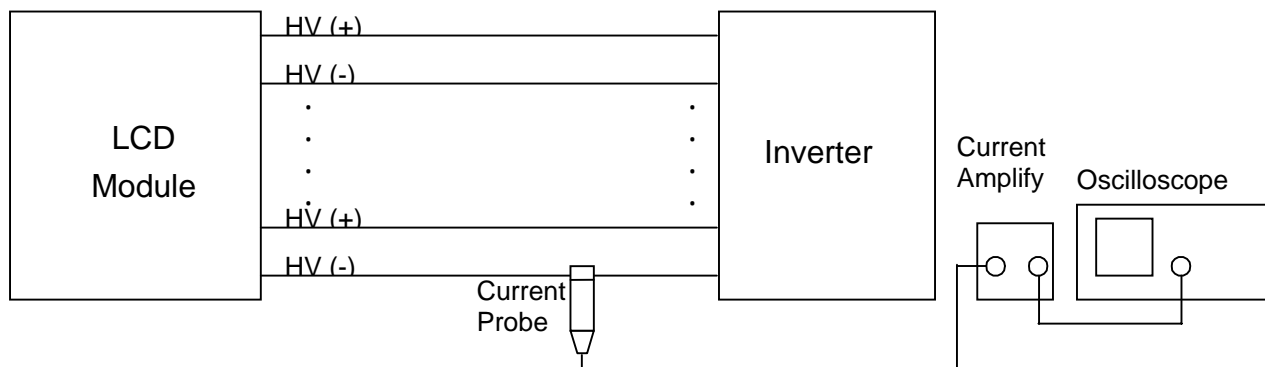
Dip condition: $4.0V \leq V_{cc} \leq 4.5V, T_d \leq 20ms$

3.3 BACKLIGHT UNIT

$T_a = 25 \pm 2^\circ C$

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	---	685	---	V_{RMS}	$I_L = 6mA$
Lamp Current	I_L	---	6.0	---	mA_{RMS}	(1)
Lamp Turn On Voltage	V_s	---	---	1510(0 °C)	V_{RMS}	(2)
		---	---	1410(25 °C)	V_{RMS}	(2)
Operating Frequency	F_L	40	---	80	KHz	(3)
Lamp Life Time	L_{BL}	50000 hr	---	---	Hrs	(5)

Note (1) Lamp current is measured by utilizing high frequency current meters as shown below:



Note (2) The voltage shown above should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) $P_L = I_L \times V_L \times 16 \text{ CCFLs}$

Note (5) The lifetime of lamp can be defined as the time in which it continues to operate under the condition

$T_a = 25 \pm 2^\circ\text{C}$ and $I_L = 2.0 \sim 5.5 \text{ mA}$ until one of the following events occurs:

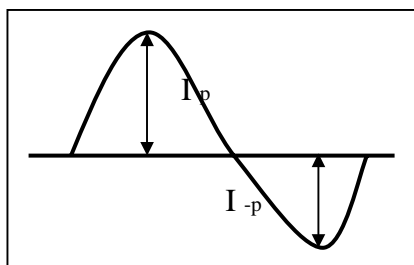
- When the brightness becomes or lower than 50% of its original value.
- When the effective ignition length becomes lower than 80% of its original value. (Effective ignition length is defined as an area that has less than 70% brightness compared to the brightness in the center point.)

Note (6) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid producing too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

The output of the inverter must have symmetrical (negative and positive) voltage waveform and symmetrical current waveform. (Unsymmetrical ratio is less than 10%) Please do not use the inverter, which has unsymmetrical voltage and unsymmetrical current and spike wave. Lamp frequency may produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

- The asymmetry rate of the inverter waveform should be 10% below;
- The distortion rate of the waveform should be within $2 \pm 10\%$;
- The ideal sine wave form shall be symmetric in positive and negative polarities.



* Asymmetry rate:

$$|I_p - I_{-p}| / I_{rms} * 100\%$$

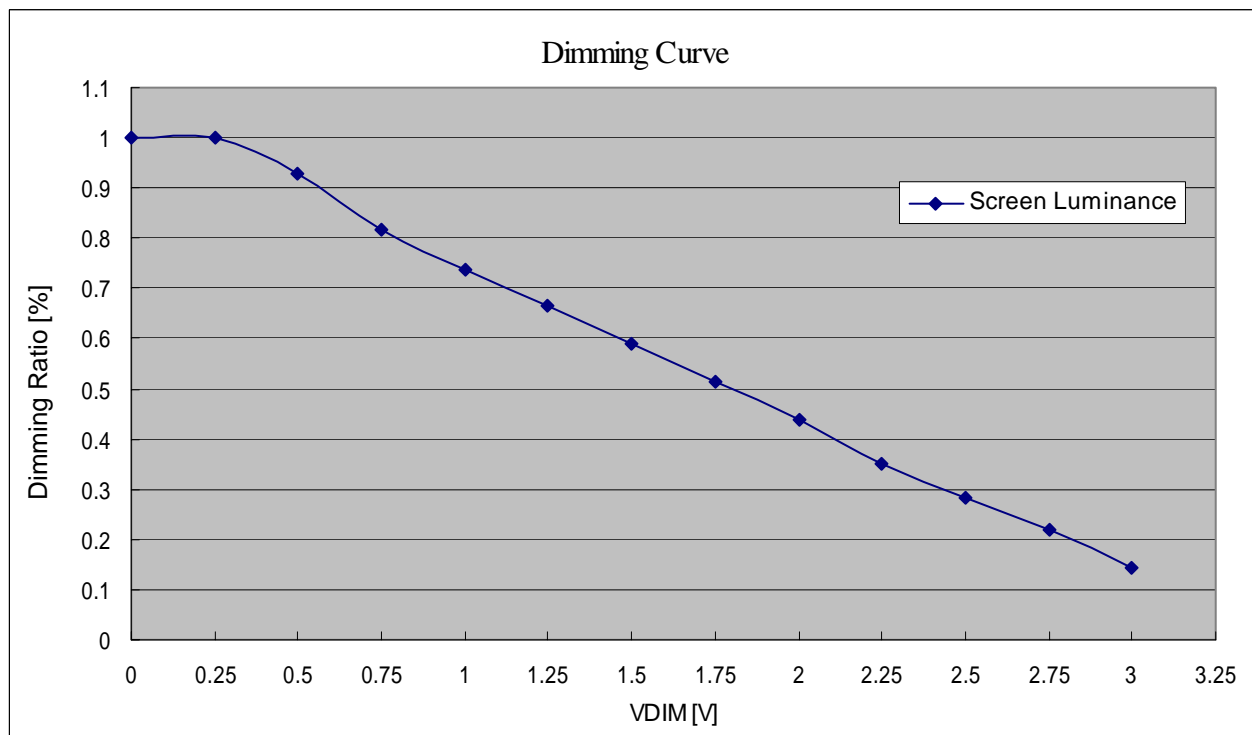
* Distortion rate

$$I_p \text{ (or } I_{-p}) / I_{rms}$$

3.3 Inverter Electrical characteristic

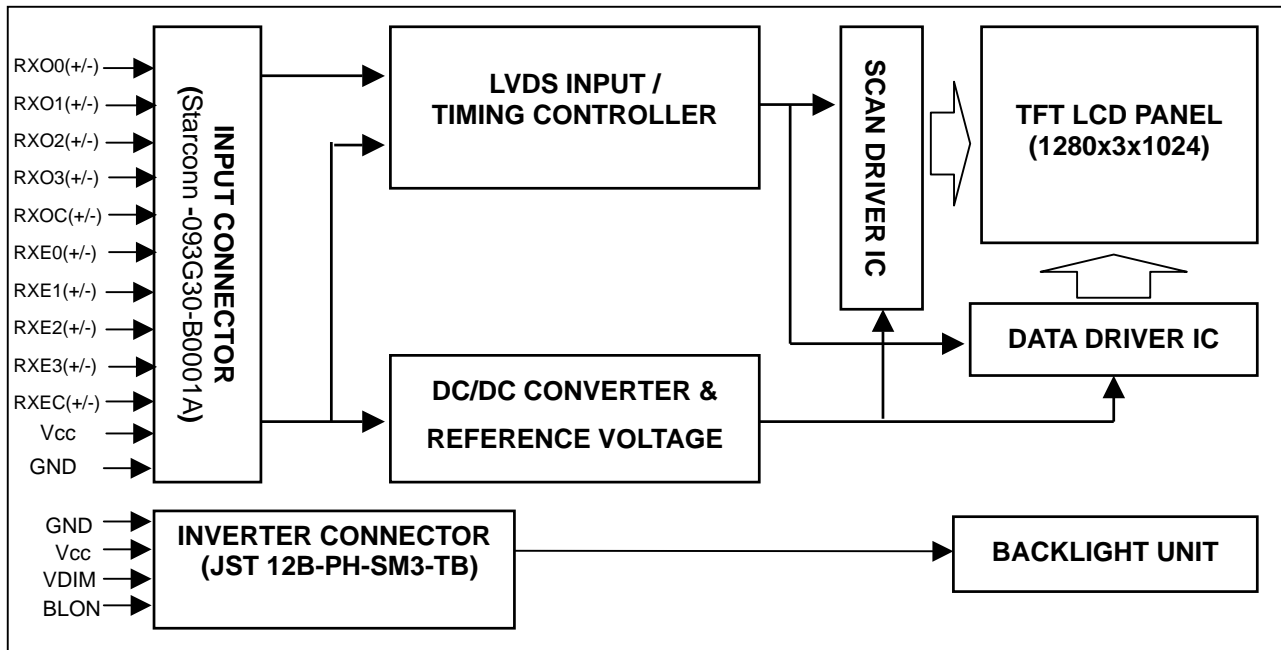
Item	Symbol	Description	Min.	Typ.	Max.	Unit
1	V_{in}	Input voltage	10.8	12	13.2	V
2	I_{in}	Input current (@ $V_{in}=12V$)	---	5	6	A
3	P_{in}	Input power	---	60	72	W
4	BLON	Inverter On/Off control: OFF	-0.1	0	0.8	V
		Inverter On/Off control: ON	2	3.3	6	V
5	VDIM	Output current control				
		VDIM: 0V, maximum brightness VDIM: 3V, minimum brightness	0	---	3	V
6	F_b	Burst Mode Frequency	225	250	275	Hz
7	Freq.	Operating frequency	45	50	55	KHz
8	I_{out}	Output current, VDIM=0V	3.7	4.2	4.7	mA
9	V_{lamp}	Lamp ignite voltage	1750	---	---	Vrms

The following chart is the VDIM vs Dimming Range for your reference.

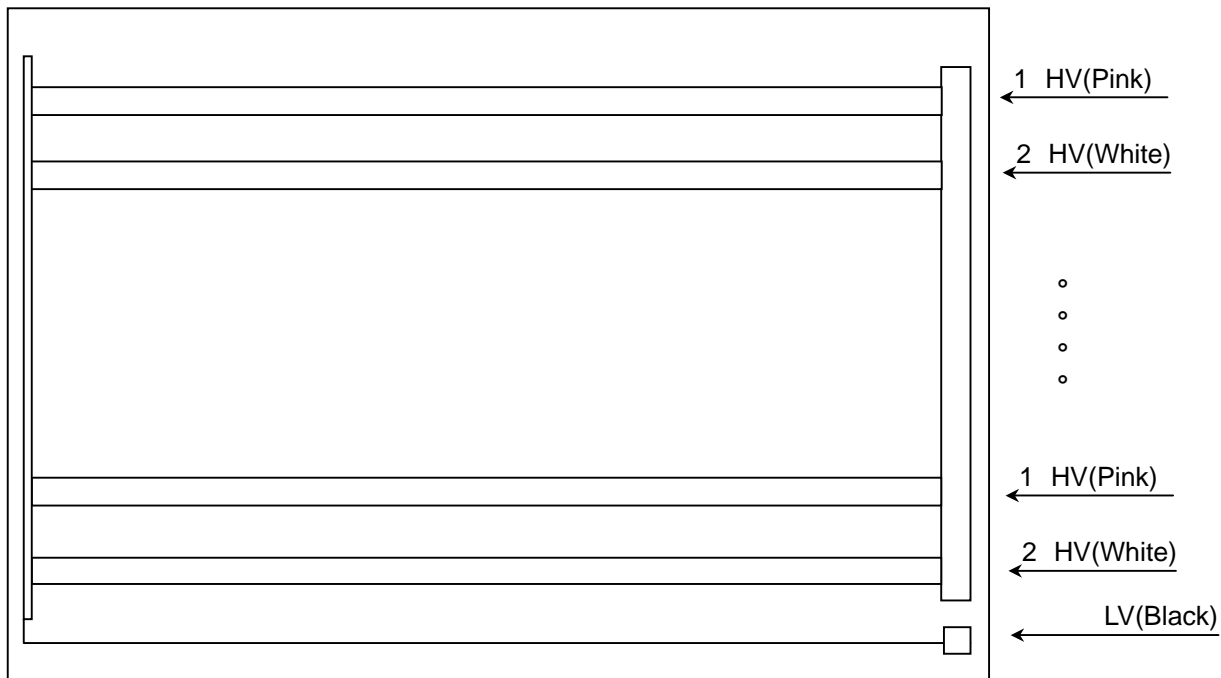


4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



4.2 BACKLIGHT UNIT



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

1	RXO0-	Negative LVDS differential data input. Channel O0 (odd)
2	RXO0+	Positive LVDS differential data input. Channel O0 (odd)
3	RXO1-	Negative LVDS differential data input. Channel O1 (odd)
4	RXO1+	Positive LVDS differential data input. Channel O1 (odd)
5	RXO2-	Negative LVDS differential data input. Channel O2 (odd)
6	RXO2+	Positive LVDS differential data input. Channel O2 (odd)
7	GND	Ground
8	RXOC-	Negative LVDS differential clock input. (odd)
9	RXOC+	Positive LVDS differential clock input. (odd)
10	RXO3-	Negative LVDS differential data input. Channel O3(odd)
11	RXO3+	Positive LVDS differential data input. Channel O3 (odd)
12	RXE0-	Negative LVDS differential data input. Channel E0 (even)
13	RXE0+	Positive LVDS differential data input. Channel E0 (even)
14	GND	Ground
15	RXE1-	Negative LVDS differential data input. Channel E1 (even)
16	RXE1+	Positive LVDS differential data input. Channel E1 (even)
17	GND	Ground
18	RXE2-	Negative LVDS differential data input. Channel E2 (even)
19	RXE2+	Positive LVDS differential data input. Channel E2 (even)
20	RXEC-	Negative LVDS differential clock input. (even)
21	RXEC+	Positive LVDS differential clock input. (even)
22	RXE3-	Negative LVDS differential data input. Channel E3 (even)
23	RXE3+	Positive LVDS differential data input. Channel E3 (even)
24	GND	Ground
25	NC	Not connection, this pin should be open
26	NC	Not connection, this pin should be open
27	NC	Not connection, this pin should be open
28	VCC	+5.0V power supply
29	VCC	+5.0V power supply
30	VCC	+5.0V power supply

Note (1) Connector Part No.: 093G30-B0001A (Starconn).

Note (2) The first pixel is odd.

Note (3) Input signal of even and odd clock should be the same timing.

Note (4) The module uses a 100-ohm resistor between positive and negative data lines of each receiver input.

5.2 LVDS DATA MAPPING TABLE

SELLVDS = Low or Open								
LVDS Channel O0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	OG0	OR5	OR4	OR3	OR2	OR1	OR0
LVDS Channel O1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	OB1	OB0	OG5	OG4	OG3	OG2	OG1
LVDS Channel O2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	OB5	OB4	OB3	OB2
LVDS Channel O3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	OB7	OB6	OG7	OG6	OR7	OR6
LVDS Channel E0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	EG0	ER5	ER4	ER3	ER2	ER1	ER0

LVDS Channel E1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	EB1	EB0	EG5	EG4	EG3	EG2	EG1
LVDS Channel E2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	EB5	EB4	EB3	EB2
LVDS Channel E3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	EB7	EB6	EG7	EG6	ER7	ER6

5.3 INVERTER INPUT SIGNAL

Pin No.	Symbol	Description
1	Vin	Input voltage
2	Vin	Input voltage
3	Vin	Input voltage
4	Vin	Input voltage
5	Vin	Input voltage
6	Gnd	Ground
7	Gnd	Ground
8	Gnd	Ground
9	Gnd	Ground
10	Gnd	Ground
11	VDIM	Brightness control (0~3V)
12	BLON	Inverter On/Off control (0/3.3V)

Note (1) Connector Part No.: S12B-PH-SM3-TB (JST) or equivalent

Note (2) User's connector Part No.: ➔ PHR-12 (JST)

5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	R7	R6	G5	G4	G3	G2	G1	G0	R7	R6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

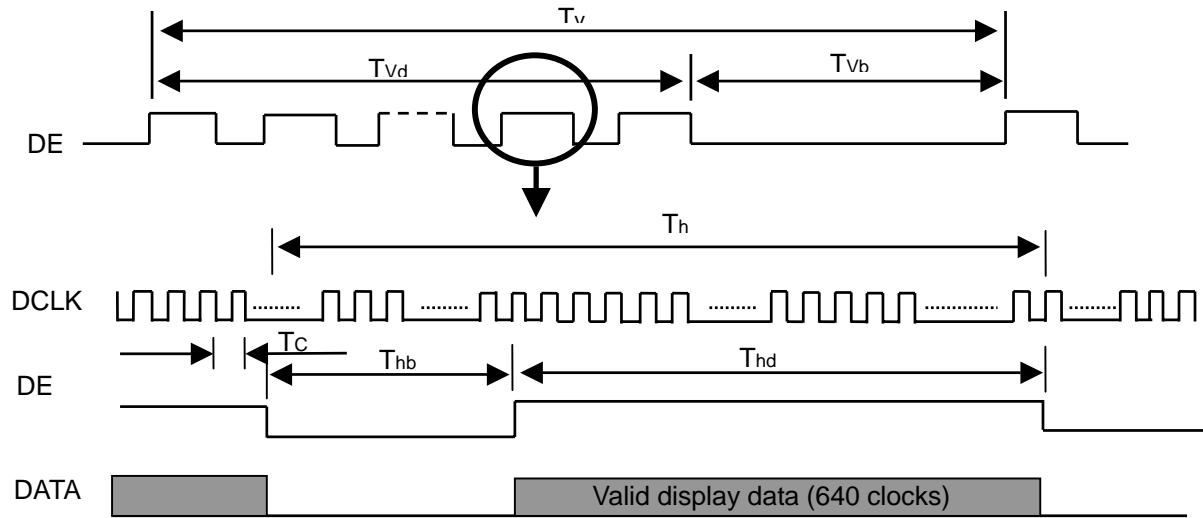
6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Clock	Frequency	Fc	-	54	67.5	MHz	-
	Period	Tc	14.8	18.5	-	ns	-
	High Time	Tch	-	4/7	-	Tc	-
	Low Time	Tcl	-	3/7	-	Tc	-
LVDS Data	Setup Time	Tlvs	600	-	-	ps	-
	Hold Time	Tlvh	600	-	-	ps	-
Vertical Active Display Term	Frame Rate	Fr	56	60	75	Hz	$T_v = T_{vd} + T_{vb}$
	Total	Tv	1034	1066	1274	Th	-
	Display	Tvd	1024	1024	1024	Th	-
	Blank	Tvb	10	42	$T_v - T_{vd}$	Th	-
Horizontal Active Display Term	Total	Th	740	844	960	Tc	$T_h = T_{hd} + T_{hb}$
	Display	Thd	640	640	640	Tc	-
	Blank	Thb	100	204	$T_h - T_{hd}$	Tc	-

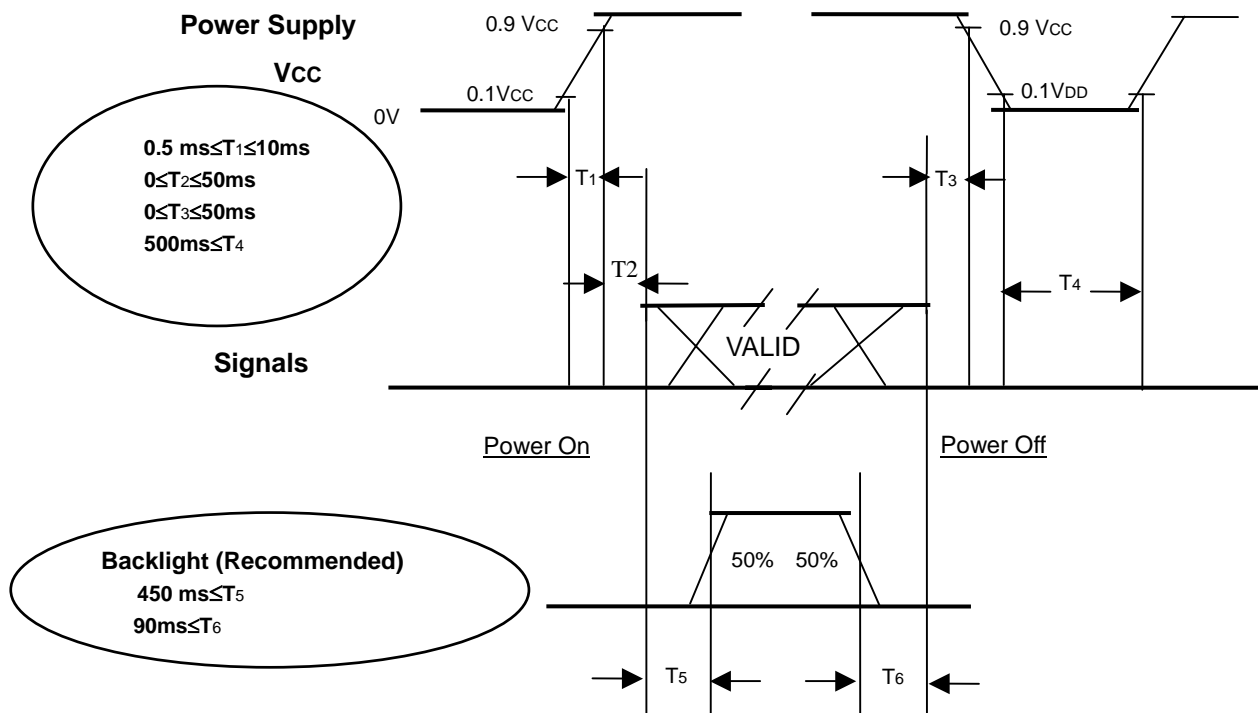
Note: Because this module is operated by DE only mode, Hsync and Vsync input signals should be set to low logic level or ground. Otherwise, this module would operate abnormally.

INPUT SIGNAL TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note.

- (1) The supply voltage of the external system for the module input should be the same as the definition of Vcc.
- (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation of the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.
- (3) In case of VCC = off level, please keep the level of input signals on the low or keep a high impedance.
- (4) T4 should be measured after the module has been fully discharged between power of and on period.
- (5) Interface signal shall not be kept at high impedance when the power is on.

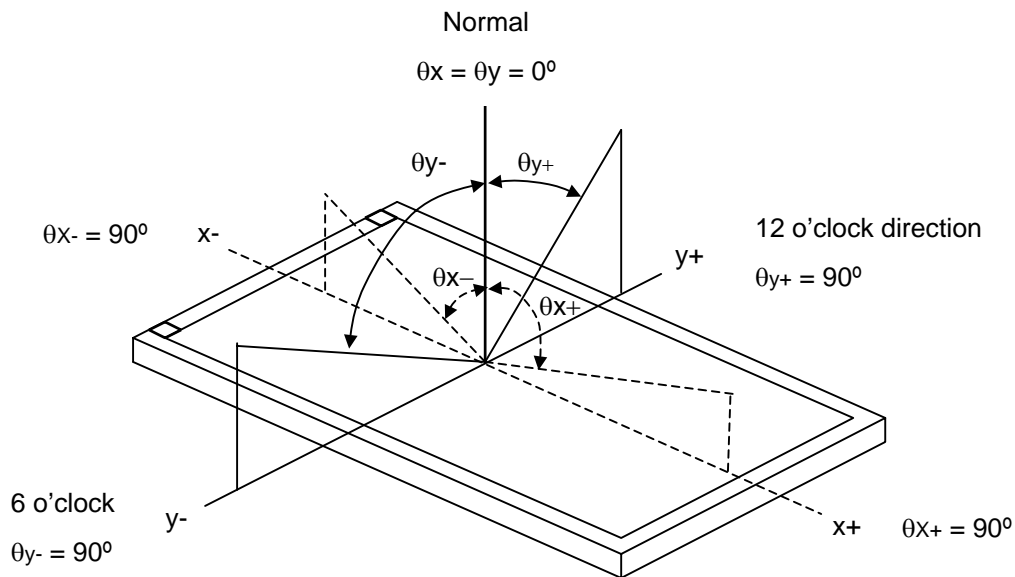
7. OPTICAL CHARACTERISTICS

7.1 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.1. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (5).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	R _x	$\theta_x=0^\circ, \theta_Y=0^\circ$ CS-1000	Typ – 0.03	0.648	Typ + 0.03		(1), (5)
		R _y			0.333			
	Green	G _x			0.284			
		G _y			0.612			
	Blue	B _x			0.150			
		B _y			0.075			
	White	W _x			0.313			
		W _y			0.329			
Center Luminance of White		L _C	500	600	---	cd/m ²	(4), (5)	
Contrast Ratio		CR	800	1000	---	-	(2), (5)	
Response Time		T _R	$\theta_x=0^\circ, \theta_Y=0^\circ$	---	5	15	ms	(3)
		T _F		---	15	25	ms	
White Variation		δW	$\theta_x=0^\circ, \theta_Y=0^\circ$ USB2000	---	1.25	1.40	-	(5), (6)
Viewing Angle	Horizontal	θ _{x+}	CR 10 USB2000	80	85	---	Deg.	(1), (5)
		θ _{x-}		80	85	---		
	Vertical	θ _{y+}		80	85	---		
		θ _{y-}		80	85	---		

Note (1) Definition of Viewing Angle (θ_x , θ_y):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{255} / L_0$$

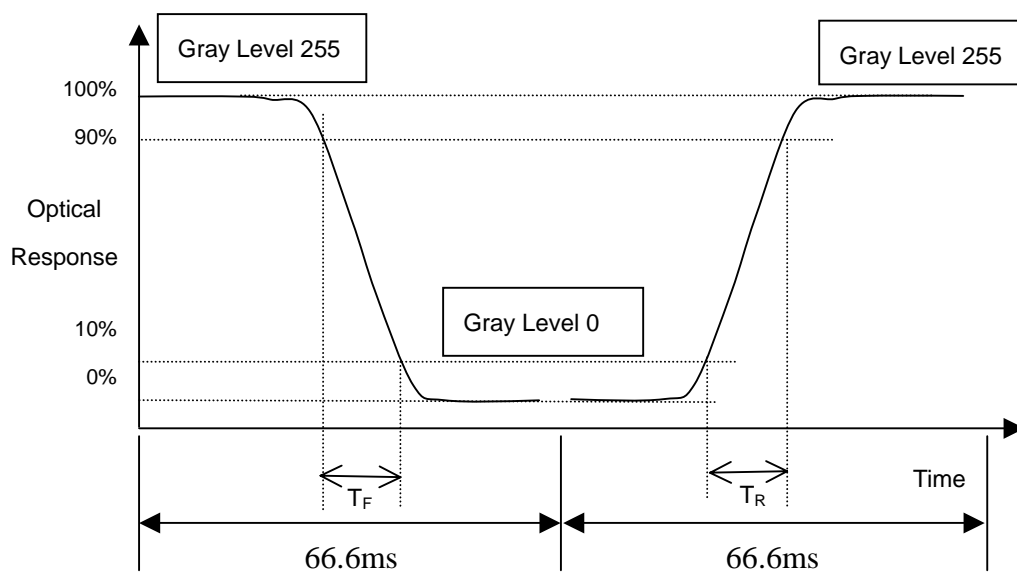
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

$$\text{CR} = \text{CR} (5)$$

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R , T_F):



Note (4) Definition of Luminance of White (L_C):

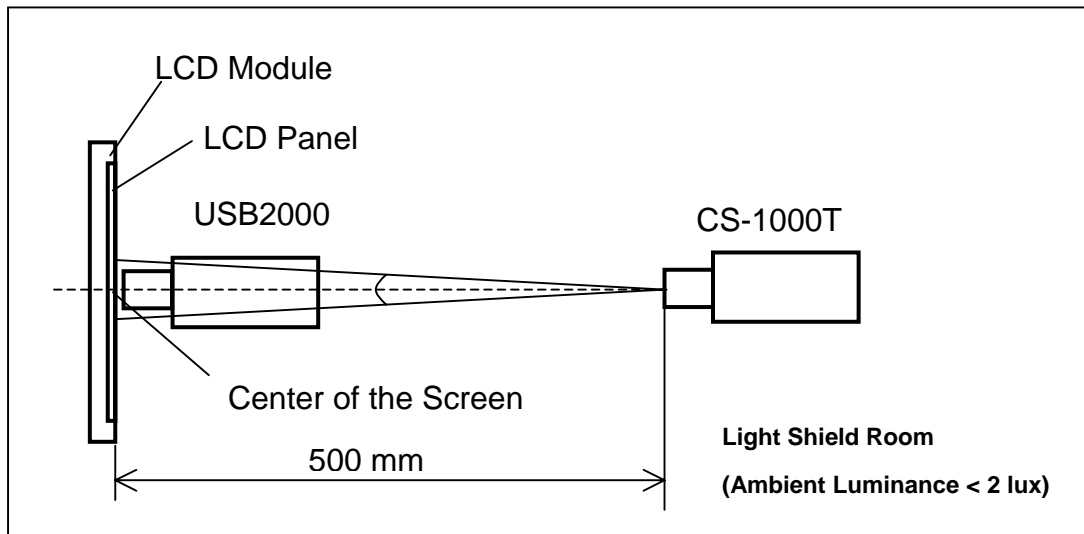
Measure the luminance of gray level 255 at center point

$$L_C = L(5)$$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (6).

Note (5) Measurement Setup:

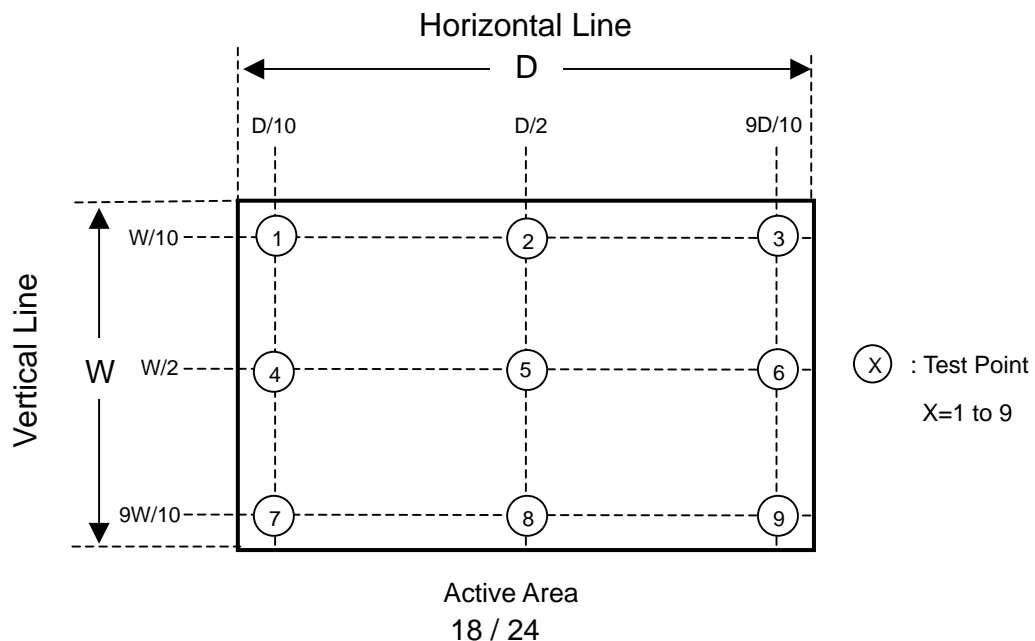
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 9 points

$$\delta W = \text{Maximum} [L(1), L(2) \dots L(4), L(9)] / \text{Minimum} [L(1), L(2) \dots L(4), L(9)]$$



8. PACKAGING

8.1 PACKING SPECIFICATIONS

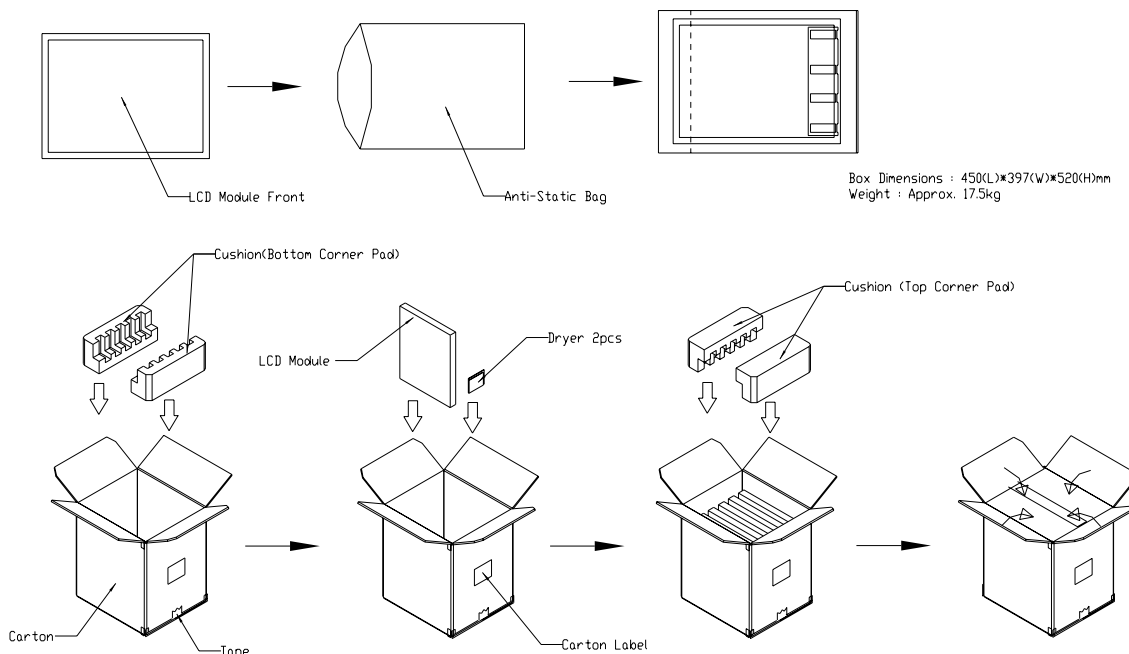
- (1) 5 LCD modules / 1 Box
- (2) Box dimensions: 450(L) X 397(W) X 520(H) mm
- (3) Weight: approximately 17.5Kg (5 modules per box)

8.2 PACKING METHOD

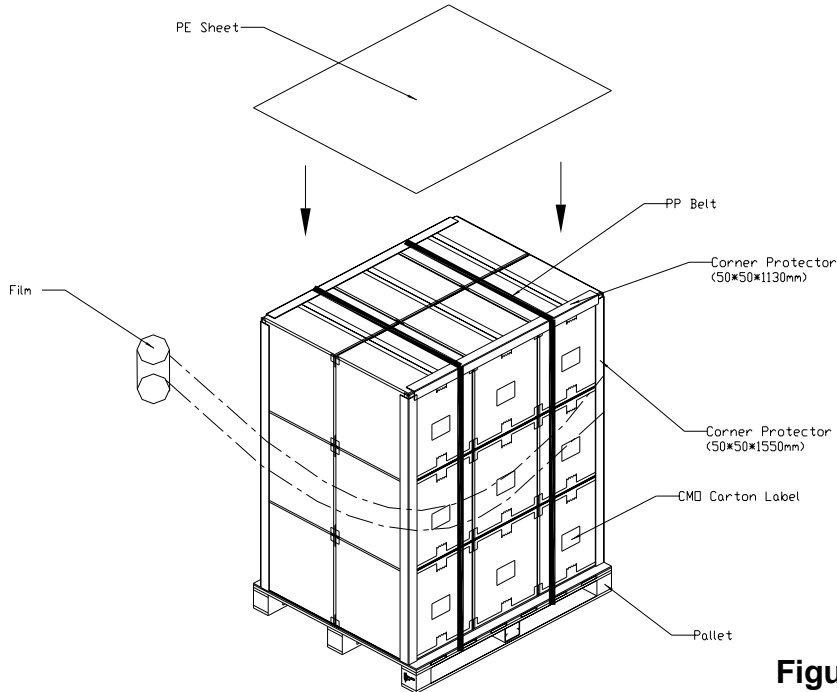
- (1) Carton Packing should have no failure in the following reliability test items.

Test Item	Test Conditions	Note
Vibration	ISTA STANDARD Random, Frequency Range: 1 – 200 Hz Top & Bottom: 30 minutes (+Z), 10 min (-Z), Right & Left: 10 minutes (X) Back & Forth 10 minutes (Y)	Non Operation
Dropping Test	1 Angle, 3 Edge, 6 Face, 60cm	Non Operation

Figure. 8-1 Packing method



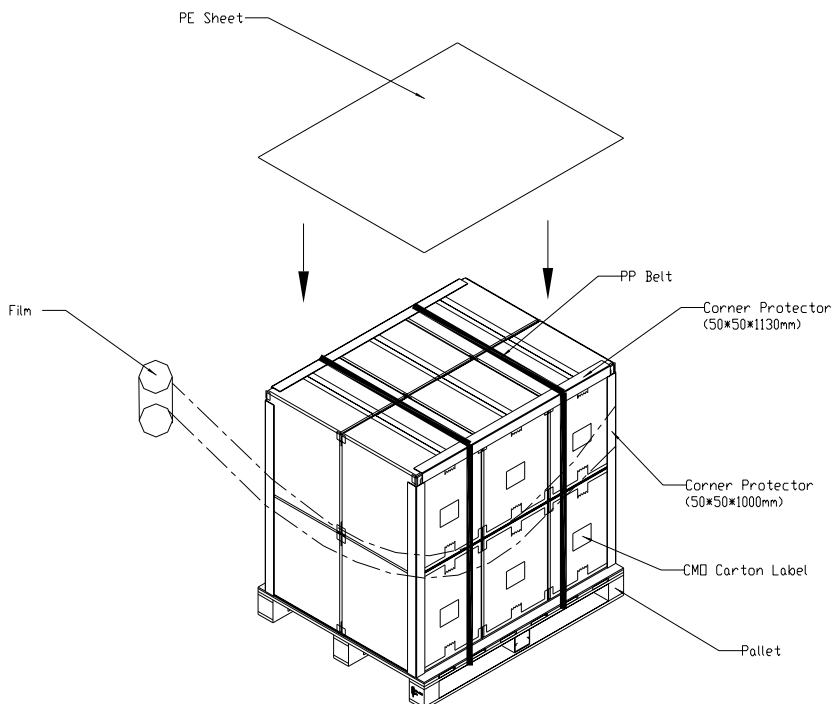
For ocean freight



NOTES:
Pallet : L1200*W1000*H135mm
Pallet Stock Dim : L1200*W1000*H1714mm

Figure. 8-2 Packing method

For air freight



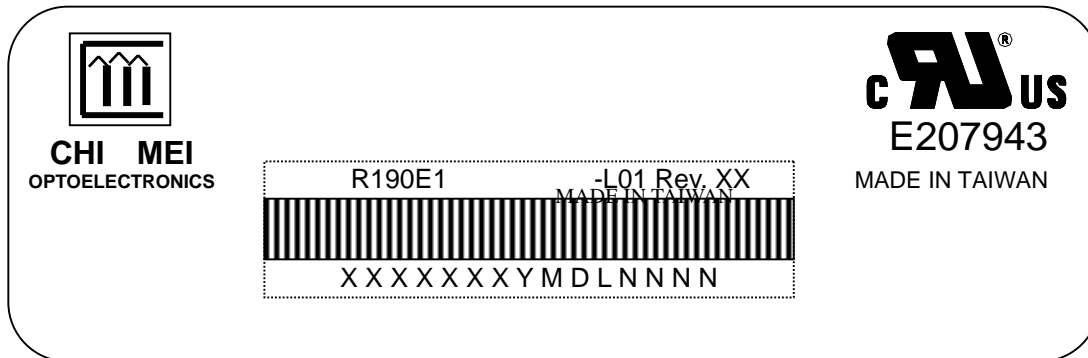
NOTES:
Pallet : L1200*W1000*H135mm
Pallet Stock Dim : L1200*W1000*H1185mm

Figure. 8-3 Packing method

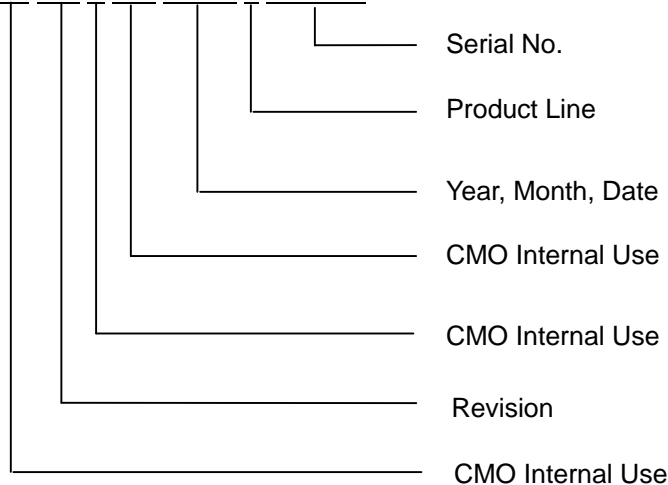
9. DEFINITION OF LABELS

9.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: R190E1 -L01
- (b) Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.
- (c) Serial ID: XXXXXXXXYMDLNNNN



Serial ID includes the information as below:

- (a) Manufactured Date: Year: 1~9, for 2000~2009
Month: 1~9, A~C, for Jan. ~ Dec.
Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.
- (b) Revision Code: Cover all the change
- (c) Serial No.: Manufacturing sequence of product
- (d) Product Line: 1 -> Line1, 2 -> Line 2, ...etc.

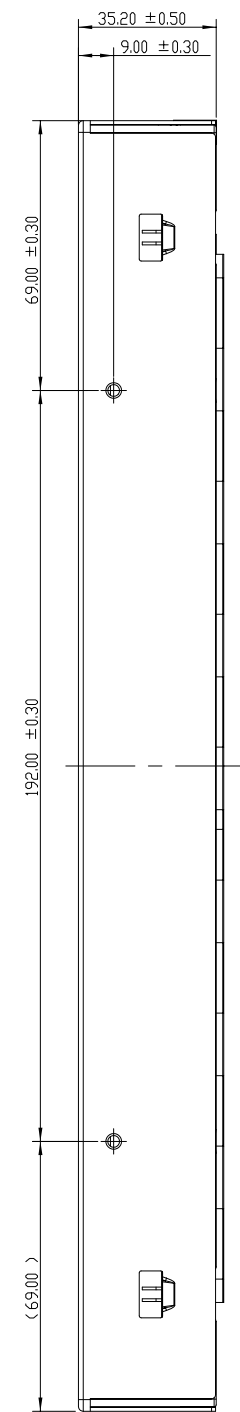
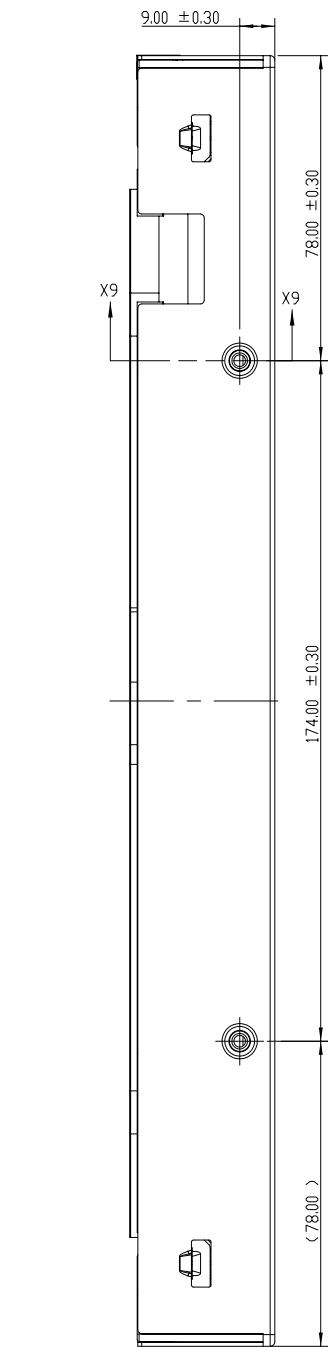
10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS



- (1) Do not apply rough force such as bending or twisting to the module during assembly.
- (2) To assemble or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) It's not permitted to have pressure or impulse on the module because the LCD panel and Backlight will be damaged.
- (4) Always follow the correct power sequence when LCD module is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.
- (5) Do not pull the I/F connector in or out while the module is operating.
- (6) Do not disassemble the module.
- (7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (8) It is dangerous that moisture come into or contacted the LCD module, because moisture may damage LCD module when it is operating.
- (9) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (10) When ambient temperature is lower than 10°C may reduce the display quality. For example, the response time will become slowly, and the starting voltage of CCFL will be higher than room temperature.

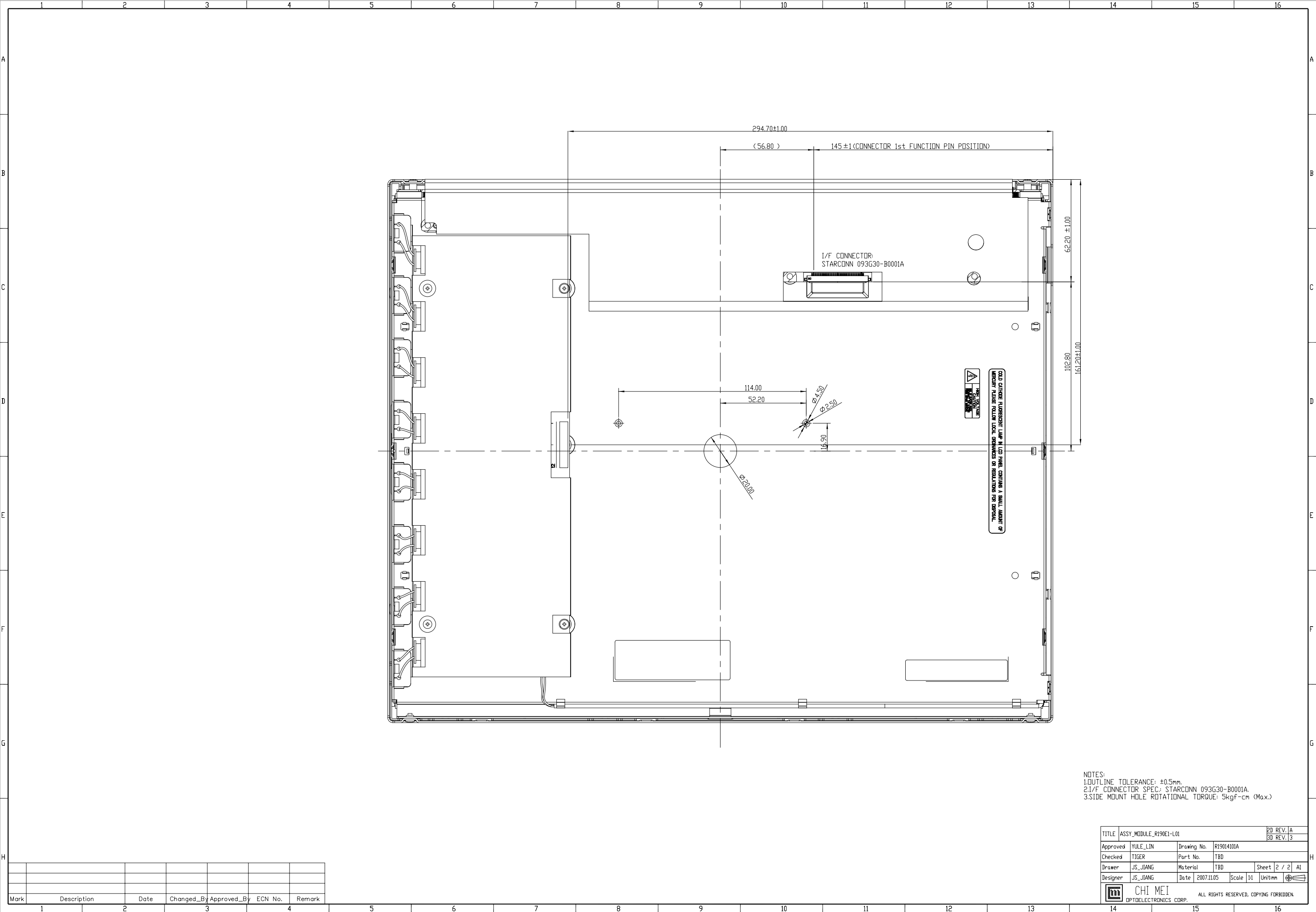
10.2 SAFETY PRECAUTIONS

- (1) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.
- (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (3) After the module's end of life, it is not harmful in case of normal operation and storage.




TITLE		ASSY_MODULE_R190E1-L01		2D REV. A	
				3D REV. 3	
Approved	YULE LIN	Drawing No.	R19014101A		
Checked	TIGER	Part No.	TBD		
Drawer	JS_JIANG	Material	TBD	Sheet	1 / 2
Designer	JS_JIANG	Date	2007.11.05	Scale	1:1
		Unit/mm			
		CHI MEI		ALL RIGHTS RESERVED, COPYING FORBIDDEN.	
		OPTOELECTRONICS CORP.			

TITLE		ASSY_MODULE_R190E1-L01		2D REV. A	
				3D REV. 3	
Approved	YULE LIN	Drawing No.	R19014101A		
Checked	TIGER	Part No.	TBD		
Drawer	JS_JIANG	Material	TBD	Sheet	1 / 2
Designer	JS_JIANG	Date	2007.11.05	Scale	1:1
		Unit/mm			
		CHI MEI		ALL RIGHTS RESERVED, COPYING FORBIDDEN.	
		OPTOELECTRONICS CORP.			



Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark
1		2		3		4

TITLE ASSY_MODULE_R190E1-L01				2D REV. 1A	
				3D REV. 13	
Approved	YULE LIN	Drawing No.	R19014101A		
Checked	TIGER	Part No.			
Drawer	JS_JIANG	Material	TBD	Sheet	2 / 2 AI
Designer	JS_JIANG	Date	2007.11.05	Scale	1:1 Unitmm
		CHI MEI			
OPTOELECTRONICS CORP.		ALL RIGHTS RESERVED, COPYING FORBIDDEN.			